**Lab 4: BJT as a Voltage Amplifier: Common Emitter mode  
   
Prerequisite:**You must have a working simulation and physical implementation of a waveform **F**unction **G**enerator that swings to both positive and negative voltages, as worked out in Lab 1 + 2. We call this the FG for short throughout the rest of this lab.   
The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.   
Settings for LTSpice: Use the following timing parameters in LTSpice simulation command

Stop time = 101m

Time to start saving data = 100m

Maximum time step = 0.01m

This skips the initial transients in the first 10ms of simulation caused by calculation artefacts, capacitive charging etc and gives you a stable picture of one full cycle of Vin @ *f~ 1kHz*

**Grand goal:**   
Design a BJT based circuit that is able to amplify a small AC input voltage to a large output Voltage. Current requirements are not very precisely defined, but the output must be able to function as a reasonably good AC voltage source (we will test in the end, how good is “reasonably” good)  
By now, you must be familiar with the terms DC voltages and currents (constant in time, with capitals V,I); AC voltages and currents (*v, i*) and the concept of “sourcing” v/s “sinking” current at a circuit node.

**Part 1) Circuit Design and Simulation [50]**

Fig 1 shows the basic structure of a voltage amplifier circuit. In principle, since *Ic = βIB → Vout = VCC – IcRC* this is all you need to crack this lab assignment!   
or… is it? NO! Some important extra components are needed to put Q1 in the proper  
operating mode as in earlier Lab, AND ensure non-linear effects  
at B-E junction are  
suppressed as given in the pre-lab reading notes.

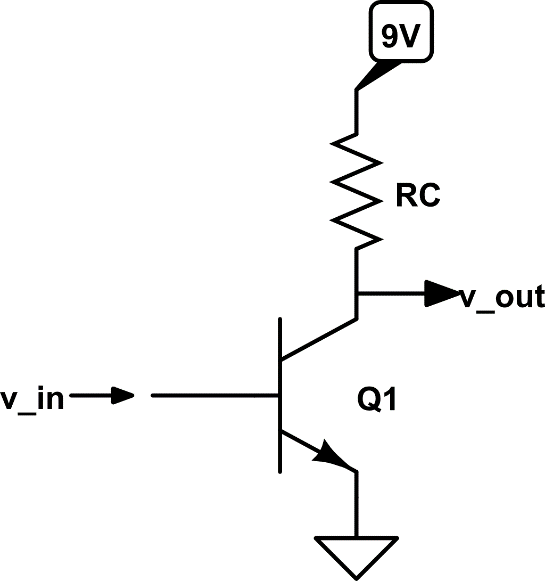


Fig 1:   
The BJT voltage amplifier… is this all there is to it?

**Level 0: The “crack”**

If vin is an AC voltage whose value can be both positive and negative,

* 1. What are the assumed conditions required for ?   
     What are the necessary absolute and relative voltage conditions required at the C, B, E terminals of Q1 to use it as a voltage amplifier? **1**

a) BJT must be in forward active mode

b) VBE = VB – V­E = 0.7V and VCB = VC – VB > 0V

* 1. Input side: Our input signal is a voltage *vin,* NOT *iin.* Is it OK to send *vin* directly into the base of Q1? Obviously not! List all the reasons why not: **1**

We wish to get the Q point current. Hence, an impedance needs to be added accordingly so that a DC Voltage is set up as a transistor bias.

**Level 1: Basic Design**

After cracking the problem concepts in Level 0, and with experience from previous circuit design, you should already have a rough idea how to proceed:  
  
The design parameters we wish to achieve in this lab are:

1. Assume VCC = 9V constant, and Q1*β* = 300
2. Use IQ = 1mA
3. Circuit gain = **–10** (note ‘–’ due to overall design)
4. Amplifier has a high-pass *f3dB* = 100 Hz
5. Test amplifier with *vin =* ± 0.3V *@* 1.17 kHz(our standard FG output)

Here is the step-by-step design procedure:

BJT terminal voltages must be setup such that it always remains in the forward-active operation mode. Here are ways in which this can be accomplished, without too much complexity:

**DC Design:**

1. Choice of IQ = 1mA  
   Note that we have chosen IQ much lower than the Q point of the emitter follower current amplifier – we are mostly interested here in voltage amplification and not too bothered about delivering large current to the load. In the first approximation, we don’t deliver *any* current to the DSO probe load. So a choice of low IQ is OK as long as we can ensure the BJT remains forward-active at all times.
2. **Calculation of RC** – we would like to allow *vout* to have maximum possible range from 0 – VCC. So, we would like to set VC at about ½ VCC. Fixing VC and IQ immediately determines RC. What value of RC do you choose? **1**

Rc = (4.5V)/(1mA) = 4500 Ω

1. **What should VE be, if it is to be?** Is it OK to connect Q1-E terminal directly to GND as shown in Fig 1? Why not?   
   *Hints:*   
   1) There is an effective *re* across B-E whose value is very small, and non-linear, dependent on temperature and *IC* : you don’t want the Q-point of the circuit (or its overall operation) to be dependent on a small non-linear *re*  
   2) VBE is ~ 0.7V in forward active mode. So VE should be at least of comparable value at the Q-point to ensure thermal stability.  
   Explain what is the Q-point value of VE required, and what is the component value required at E? [listed in pre-reading notes] **3**  
   No, we cannot connect Q1-E terminal directly to GND in order to avoid the transistor going into saturation or cutoff. Another reason is to avoid the non-linear effect of re, i.e. to avoid the increase in its resistance value cause by thermal heating.

We set VEQ = 0.1Vcc. Hence in this case, VE = 0.9V.  
  
  
  
**Finer points of choosing VEQ: 2***Setting VE to be 0.1VCC directly, you will find that you don’t get to gain   
G= – 10 in step 5 below. So you can come back here to re-do the VEQ setting to lower than 0.1VCC (while still having dominate over re) – Design is an iterative process!*VEQ = 0.05VCC

1. **Setting VB:** Once DC values of VC  and VE are decided in steps above, choose the simplest method of setting VB (similar considerations as used in earlier current amplifier lab apply, to make sure the biasing network provides a much lower impedance path to ground than RB.   
   List the values of components used to set VB here: **2**

RB1 = 22kΩ and RB2 = 3.3kΩ

VB = VCCRB2/(RB1+RB2)

1. **What AC voltage gain do you get?**   
   Combining the answers to questions 2 & 3 gives you the AC voltage gain of the amplifier.Note: Though we are technically in the DC design phase, we are looking ahead and interested in the AC voltage gain. So turn all the capital letter quantities V…, I… into small case and do a little bit of math with the AC terms *vin=vB, vC=vout,* *iC, iE, iB*.   
   The main steps involve using the fact that  
   *vout = vC = –iCRC* (VCC is DC value drops out) &  
   *re ≪ RE* by design *vB = vE* since *VBE = 0.7V* is fixed by the DC design.  
   You may find, surprisingly, that *β* is not involved in the final voltage gain of this circuit!   
    **5**

Vout/Vin = -RC/(re+RE)

Now, re = 25mV/IQ = 25Ω

Therefore, Vout/Vin = -4500/(355) = -12.5  
  
 **AC Design:**

1. Input side: In general *Vin = Vin|dc + vin*. We want to strictly reject Vin|dc hence the 100Hz f3dB high pass filter at the input is required. Calculate the value of the required component. The calculation is similar to the way we used *Rinp* of the amplifier as part of the CR high-pass filter in earlier lab **1**Rin = 742 Ω

C = 1/(2πfRin) = 3.3µF (approx.)

1. Output side: we are interested in only amplifying the AC component of *IC = IQ+iC* In fact,  we want to *block* any DC share of the current flowing through *RC* getting diverted to the load – this will disturb our DC calculations above!  
   Calculate the filter components required at the output before connecting to *vout*­What is the corresponding R required for this filter calculation? Recall from the reading notes that looking back Q1’s C, the CB junction is effectively open circuit (MΩ) and there is only one other resistor at that junction! **1**R\_load = 75kΩ

C = 4.7µF

**Go back and check:** you may now realize that as long as you keep Q1 in forward-active mode, some IQ and hence a DC IB = IQ/β is required. Since IQ has been set very low, corresponding DC IB must be really small indeed! This means you must obey the constraint (RB1||RB2)≪RB much more strictly to make sure most of the DC current in the biasing path is preferentially sent into the biasing network and *not* into the base of Q1. Re-check your answers to question 4) in the DC design above for the biasing network to set VB to make sure your design is self-consistent in terms of all the DC values and the design gain G is achieved.

**1**

**Level 3: Advanced Design check 2**

Is the gain constant over the full span of *vin = ± 0.3V*?

We have designed for a gain of G= –10 at the Q-point. But as *vin* varies *iC* varies around ICQ *and hence re also changes.*  Have you chosen your component values conservatively enough that for the given design parameters, *G = –10* is constant?

No, the gain is not constant over the full span of *vin = ± 0.3V*

**Level 4: Simulate in LTSpice and plot 30**

Simulate the complete circuit as designed above in LTSpice and check its performance as per the design parameters

(*vin = ±0.3V, f=1.17kHz, Gain = –10*)

Put your LTSpice circuit diagram and simulation result plots below.

Make sure to plot voltages as a function of time (as you will check them after building the circuit). Also, plot voltages *vout v/s vin* to check the Gain linearity and any peculiar features.

